The opinion in support of the decision being entered today was <u>not</u> written for publication and is <u>not</u> binding precedent of the Board.

Paper No. 15

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte TONIA G. MORRIS

Application No. 09/072,758

ON BRIEF

Before GROSS, BARRY, and BLANKENSHIP, <u>Administrative Patent Judges</u>. BLANKENSHIP, <u>Administrative Patent Judge</u>.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 1-4 and 8-19.

We affirm-in-part.

BACKGROUND

The invention is directed to an image sensing array (ISA) having discrete and continuous time processing capabilities. Representative claims 1 and 14 are reproduced below.

1. An apparatus comprising:

a light sensitive element that generates a photocurrent related to an incident light level;

an integration circuit coupled to the light sensitive element to compute an average of the photocurrent during a sampling period to permit creation of a digital image; and

a continuous time processing circuit coupled to the light sensitive element to receive and process the photocurrent during at least a continuous segment of time, the continuous time processing interpreting an aspect of the digital image.

14. A system comprising:

an image sensing array (ISA) having a plurality of pixels that form a focal plane, the ISA having both continuous time processing capability and integration capability, the continuous time processing to interpret an aspect of an image; and

a memory coupled to the ISA to store a representation of an image corresponding to light levels on a surface of the ISA during a sampling period.

The examiner relies on the following references:

Horn et al. (Horn)	5,220,398	Jun. 15, 1993
Standley	5,572,074	Nov. 5, 1996
Brajovic	5,699,278	Dec. 16, 1997 (filed Jan. 24, 1995)

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Kramer 5,998,780 Dec. 7, 1999 (filed Feb. 26, 1998)

K. Aizawa et al. (Aizawa), <u>On Sensor Image Compression For High Pixel Rate Imaging</u>, Proceedings of the 1996 IEEE/SICE/RSJ International Conference on Multisensor Fusion and Integration for Intelligent Systems, pp. 201-207 (1996).

S. Kawahito et al. (Kawahito), <u>CMOS image sensors with video compression</u>, Design Automation Conference 1998, Proceedings of the ASP-DAC '98, Asia and South Pacific, pp. 595-600 (Feb. 1998).

Claim 14 stands rejected under 35 U.S.C. § 102 as being anticipated by Aizawa.

Claims 1-3, 8, 9, 11-14, and 16 stand rejected under 35 U.S.C. § 102 as being anticipated by Brajovic.

Claims 15 and 18 stand rejected under 35 U.S.C. § 103 as being unpatentable over Aizawa and Kawahito.

Claims 15-18 stand rejected under 35 U.S.C. § 103 as being unpatentable over Brajovic and Kawahito.

Claim 4 stands rejected under 35 U.S.C. § 103 as being unpatentable Brajovic and Kramer.

Claims 10 and 19 stand rejected under 35 U.S.C. § 103 as being unpatentable over Brajovic and Horn.

Claim 19 stands rejected under 35 U.S.C. § 103 as being unpatentable over Brajovic and Standley.

Claims 5-7 have been objected to as depending from rejected base claim 1.

We refer to the Final Rejection (Paper No. 6) and the Examiner's Answer (Paper No. 12) for a statement of the examiner's position and to the Brief (Paper No. 11) and the Reply Brief (Paper No. 13) for appellant's position with respect to the claims which stand rejected.

OPINION

Claim 14, Section 102 rejection over Aizawa

The examiner sets forth the rejection of claim 14 as being anticipated by Aizawa on pages 5 and 6 of the Answer. Appellant's position (Brief at 8-9) is that Aizawa fails to disclose or suggest a continuous time processing capability to interpret an aspect of an image. According to appellant, the "compression sensor" of Aizawa uses discrete time processing to process detected image signals.

In response, the examiner reiterates (Answer at 15-17) that Aizawa's disclosure of using an analog circuit for the processing of each pixel is deemed to read on the broadly claimed "continuous time processing to interpret an aspect of an image."

Further, the examiner finds that Figures 5 and 7 of Aizawa disclose operational amplifiers for processing analog signals -- or for "continuous time processing." Further, the examiner reasons that Aizawa's teaching of the imaging sensor corresponding to a retina -- biological vision -- requires that analog signals generated by the photodiode be continuously processed to correctly detect motion or movement (i.e., an aspect) of an image.

Appellant's arguments do not persuade us that the examiner's finding of anticipation is in error. In particular, while Aizawa may disclose "discrete time processing" of image signals, appellant has not explained why the analog signal processing disclosed by Aizawa may not be considered "continuous time processing" as claimed. Further, we note that while instant claim 14 requires continuous time processing capability, the claim does not preclude discrete time processing in addition to the continuous time processing capability. That is, for all the claim requires, there may be continuous time processing of an image signal, the processed signal sampled, and discrete time (digital) processing with respect to the sampled signal.

Appellant argues (Reply Brief at 4) there is no teaching or suggestion in Aizawa of the system as claimed, having both integration capability to perform integration of photocurrent during a sampling period and continuous time processing capability to process continuously varying photocurrent to interpret an aspect of an image.

Appellant's arguments are not commensurate with the scope of instant claim 14. The claim does not require integration of a photocurrent during a sampling period. Aizawa describes "integration of sensing and compression" (e.g., p. 201, col. 1). Claim 14 as drafted requires little of the "integration capability" but its presence -- i.e., only that the "capability" is one of the characteristics of the ISA -- and so fails also to distinguish over the reference's disclosure of integrating sensing and compression.

We therefore sustain the rejection of claim 14 under 35 U.S.C. § 102 as being anticipated by Aizawa.

Claims 1-3, 8, 9, 11-13, and 16, Section 102 rejection over Brajovic

The statement of the rejection of claims 1-3, 8, 9, 11-13, and 16 (Answer at 7) asserts that Brajovic discloses a "light sensitive element" 12 and 30, an "integration circuit" 60, 12, and a "continuous time processing circuit" 90, 40.

Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim. <u>Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.</u>, 730 F.2d 1452, 1458, 221 USPQ 481, 485 (Fed. Cir. 1984). We cannot sustain the rejection of claim 1 as being anticipated by Brajovic.

Brajovic discloses a radiation sensitive control element 60, which includes a photodiode 12. Col. 5, II. 49-54; Fig. 2. Radiation control element 60 and local processor 90 together make up circuit 30 of Figure 2. Col. 5, II. 1-30. The rejection thus contemplates that the "integration circuit" makes up part of the "light sensitive element," and that photodiode 12 is common to both the circuit and the element. Instant claim 1, however, recites, inter alia, "an integration circuit coupled to the light sensitive element," and thus requires separate elements to perform the claimed functions. We agree with appellant that Brajovic cannot support a finding of anticipation with respect to the subject matter of claim 1, at least for the reason that each and every element of the claim has not been shown as described by the reference.

The rejection of claim 1 also refers to embodiments other than that shown in Figures 1 and 2 of the reference, and thus not to elements arranged as in the claim.

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The photodiode 12 in the embodiment of Figure 2 operates in "the photon-flux-integrating mode." Col. 6, II. 10-33. The disclosure at the bottom of column 12, teaching that the sensor "may provide continuous instantaneous measurement of the received radiation," appears to refer to possible alternatives to the embodiments of Figures 1 through 4, in view of the description preceding the teaching.

In relation to the above-noted disclosure of "continuous instantaneous measurement," we also agree with appellant that the claimed continuous time processing circuit "to receive and process the photocurrent" from the light sensitive element has not been shown in Brajovic. The rejection relies, in part, on the reference's disclosure at column 8, lines 7 through 18 that "[t]he generated data stream may be at least one analog waveform." The waveform is generated by global processor 40 (Fig. 6). The section thus describes a generated output, rather than processing of photocurrent from a light sensitive element.

Figure 5 of Brajovic, on the other hand, appears to shows an analog waveform, which is an input signal to memory 70 (Fig. 2), but not generated by the photosensitive element. As described in columns 6 and 7 of the reference, when the voltage of the photodiode 12 approaches the threshold of inverter 10, the inverter's output changes from low to high. Any "continuous time" receiving and processing of photocurrent appears to be related to the integration of the photocurrent; i.e., the "Sensor Signal" shown in Figure 5. Instant claim 1, however, requires a separate "integration circuit"

and "continuous time processing circuit," each coupled to the light sensitive element and operating on photocurrent generated by the light sensitive element.

Instant method claim 9 requires separate steps of integrating the plurality of photocurrents and performing continuous time processing on the plurality of photocurrents. We agree with appellant that the rejection fails to show these separate steps, within the same process, in Brajovic.

In view of the claims incorporating the limitations of independent claim 1 or independent claim 9, we do not sustain the rejection of claims 1-3, 8, 9, 11-13, and 16 under 35 U.S.C. § 102 as being anticipated by Brajovic.

Claim 14, Section 102 rejection over Brajovic

We will sustain the rejection of claim 14 as being anticipated by Brajovic.

Appellant argues (Brief at 13) that the examiner erred in concluding that Brajovic discloses both continuous time processing capability and integration capability. Instant claim 14, however, does not require that the continuous time processing and integration capability be mutually exclusive.

As we noted <u>supra</u>, in our review of the teachings of Brajovic, photodiode 12 operates in a photon-flux-integrating mode that integrates the incident light signal as it is received in continuous time; i.e., without sampling circuitry in the embodiment of

Figure 2.¹ That Brajovic may disclose, as appellant argues, circuitry that counts events or detects changes in histogram patterns -- <u>subsequent to</u> the processing of photocurrent at photodiode 12 -- is essentially irrelevant in view of the scope of instant claim 14.

Claims 15 and 18, Section 103 rejection over Aizawa and Kawahito

Appellant's argument in support of claims 15 and 18 (Brief at 13-15), other than the alleged deficiencies in Aizawa that we have found to be unpersuasive, is the asserted lack of suggestion or motivation in either reference of compression responsive to continuous time processing.

Appellant's position appears to presuppose that Aizawa lacks continuous time processing -- a postulate that we find untenable. In any event, we agree with the examiner's position set out in the Answer. Moreover, the compression engine taught by Kawahito is for compressing image data prior to storage. The compression engine would have no data to compress, absent completion of processing of the image signal by the ISA, or upon "a result" of continuous time processing within the ISA, as recited in instant claim 15.

Being unpersuaded of error in the rejection, we sustain the Section 103 rejection of claims 15 and 18 over Aizawa and Kawahito.

¹ Brajovic describes an alternative embodiment (Fig. 4) that includes a shutter 4 for enabling discrete sampling periods. Col. 10, II. 11-40.

Claims 15-18, Section 103 rejection over Brajovic and Kawahito

We find no separate arguments from appellant in response to the Section 103 rejection of claims 15-18 over Brajovic and Kawahito. Appellant thus relies on the arguments in support of base claims 9 and 14.

We refer to the examiner's findings in support of the rejection of claims 15 and 18, and sustain the rejection. However, since claims 16 and 17 incorporate the limitations of claim 9, and Kawahito as applied fails to remedy the deficiencies of Brajovic as applied against claim 9, we do not sustain the rejection of claims 16 and 17.

Claims 4, 10, and 19

We do not sustain the Section 103 rejections of claim 4, 10, or 19. Neither Kramer, Horn, nor Standley as applied remedy the deficiencies in Brajovic as applied against base claim 1 or 9.

CONCLUSION

The rejection of claim 14 under 35 U.S.C. § 102 as being anticipated by Aizawa is affirmed. The rejection of claim 14 under 35 U.S.C. § 102 as being anticipated by Brajovic is affirmed. The rejection of claims 15 and 18 under 35 U.S.C. § 103 as being unpatentable over Aizawa and Kawahito is affirmed. The rejection of claims 15 and 18 under 35 U.S.C. § 103 as being unpatentable over Brajovic and Kawahito is affirmed.

The rejection of claims 1-3, 8, 9, 11-13, and 16 under 35 U.S.C. § 102 as being anticipated by Brajovic is reversed. The rejection of claims 16 and 17 under 35 U.S.C. § 103 as being unpatentable over Brajovic and Kawahito is reversed. The rejection of claim 4 under 35 U.S.C. § 103 as being unpatentable over Brajovic and Kramer is reversed. The rejection of claims 10 and 19 under 35 U.S.C. § 103 as being unpatentable over Brajovic and Horn is reversed. The rejection of claim 19 under 35 U.S.C. § 103 as being unpatentable over Brajovic and Standley is reversed.

The examiner's decision in rejecting claims 1-4 and 8-19 is thus affirmed-in-part.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

ANITA PELLMAN GROSS Administrative Patent Judge)))
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